National Semiconductor

T-46-13-27

NMC9314B 1024-Bit Serial Electrically Erasable Programmable Memory

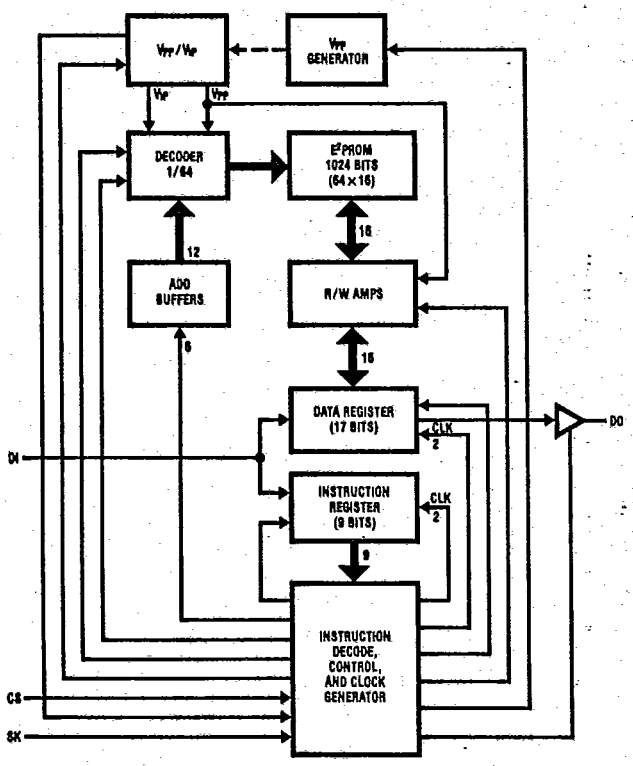
General Description

The NMC9314B is a 1024-bit non-volatile, sequential E²PROM, fabricated using advanced N-channel E²PROM technology. It is an external memory with the 1024 bits of read/write memory divided into 64 registers of 16 bits each. Each register can be serially read or written by a COP400 controller, or a standard microprocessor. Written information is stored in a floating gate cell until updated by an erase and write cycle. The NMC9314B has been designed for applications requiring up to 10^4 erase/write cycles per register. A power-down mode is provided by CS to reduce power consumption by 75 percent.

Features

- 10,000 erase/write cycles
- 10 year data retention
- Low cost
- Single supply read/write/erase operations (5V ± 10%)
- TTL compatible
- 64 x 16 serial read/write memory
- MICROWIRE™ compatible serial I/O
- Simple interfacing
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology
- Self-timed programming cycle
- Device status signal during programming

Block and Connection Diagrams



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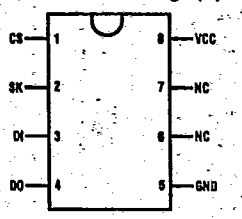
Dual-In-Line Package (N)



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Top View

Order Number NMC9314N
See NS Package N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage Relative to GND	+6V to −0.3V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temp.	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Rating	>2000V

DC and AC Electrical Characteristics $0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\%$ unless specified

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Operating Voltage		4.5	5.5	V
I_{CC1}	Operating Current Erase/Write Operating Current	$V_{CC}=5.5V$, CS=1, SK=1 $V_{CC}=5.5V$		17 17	mA mA
I_{CC2}	Standby Current	$V_{CC}=5.5V$, CS=0		5	mA
	Input Voltage Levels				
V_{IL}			−0.1	0.8	V
V_{IH}			2.0	$V_{CC}+0.5$	V
	Output Voltage Levels				
V_{OL}		$I_{OL}=2.1$ mA		0.4	V
V_{OH}		$I_{OH}=-400\ \mu A$	2.4		V
I_{LI}	Input Leakage Current	$V_{IN}=5.5V$		10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=5.5V$, CS=0		10	μA
	SK Frequency		0	200	kHz
t_{SKH}	SK High Time (Note 2)		3		μs
t_{SKL}	SK Low Time (Note 2)		2		μs
	Inputs				
t_{CSS}	CS		0.2		μs
t_{CSH}			0		μs
t_{DIS}	DI		0.4		μs
t_{DIH}			0.4		μs
	Output	$C_L=100$ pF			
t_{pd1}	DO	$V_{OL}=0.8V$, $V_{OH}=2.0V$		2	μs
t_{pd0}		$V_{IL}=0.45V$, $V_{IH}=2.40V$		2	μs
$t_{E/W}$	Self-Timed Program Cycle			15	ms
t_{CS}	Min CS Low Time (Note 3)		1		μs
t_{SV}	Rising Edge of CS to Status Valid	$C_L=100$ pF		1	μs
t_{0H}, t_{1H}	Falling Edge of CS to DO TRI-STATE®			0.4	μs

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 5 μs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 5 μs. e.g., if $t_{SKL} = 2$ μs then the minimum $t_{SKH} = 3$ μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Instruction Set for NMC9314B

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5A4A3A2A1A0		Read register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15–D0	Write register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0		Erase register A5A4A3A2A1A0
EWEN	1	00	11xxxx		Erase/write enable
EWDS	1	00	00xxxx		Erase/write disable
ERAL	1	00	10xxxx		Erase all registers
WRAL	1	00	01xxxx	D15–D0	Write all registers

NMC9314B has 7 instructions as shown. Note that the MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for 1 of 64, 16-bit registers.

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Functional Description

The NMC9314B is a small peripheral memory intended for use with COPS™ controllers and other nonvolatile memory applications. Its organization is sixty-four registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, two bits as an op code, and six bits of address. The programming cycle is self-timed, with the data out (DO) pin indicating the ready/busy status of the chip. The on-chip programming voltage generator allows the user to use a single power supply (V_{CC}). It only generates high voltage during the programming modes (write, erase, chip erase, chip write). The DO pin is valid as data out during the read mode, and if initiated, as a ready/busy status indicator during a programming cycle. During all other modes the DO pin is in TRI-STATE, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a read instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

When V_{CC} is applied to the part it powers up in the programming disable (EWDS) state, programming must be preceded by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed or V_{CC} is removed from the part. The programming disable instruction is provided to protect against accidental data disturb. Execution of a read instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMs, the register must first be erased (all bits set to logical '1') before the register can be written (certain bits set to logical '0'). After an erase instruction is input, CS is dropped low. This falling edge of CS determines the start of the self-timed programming cycle. If CS is brought high subsequently (after observing the t_{CS} specification), the DO pin will indicate the ready/busy status of the chip. The DO pin will go low if the chip is still programming. The DO pin will go high when all bits of the register at the address specified in the instruction have been set to a logical '1'. The part is now ready for the next instruction sequence.

WRITE (Note 4)

The write instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (D0) is put on the data in (DI) pin CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. Like all programming modes, DO indicates the ready/busy status of the chip if CS is brought high after a minimum of 1 μS (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction. The register to be written into must have been previously erased.

CHIP ERASE (Note 4)

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a logical '1'. Each register is then ready for a write instruction. The chip erase cycle is identical to the erase cycle except for the different op code.

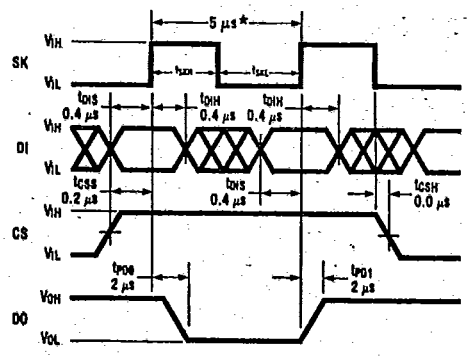
CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the self-timed programming cycle and status check.

Timing Diagrams

Synchronous Data Timing



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*This is the minimum SK period.

Timing Diagrams (Continued)

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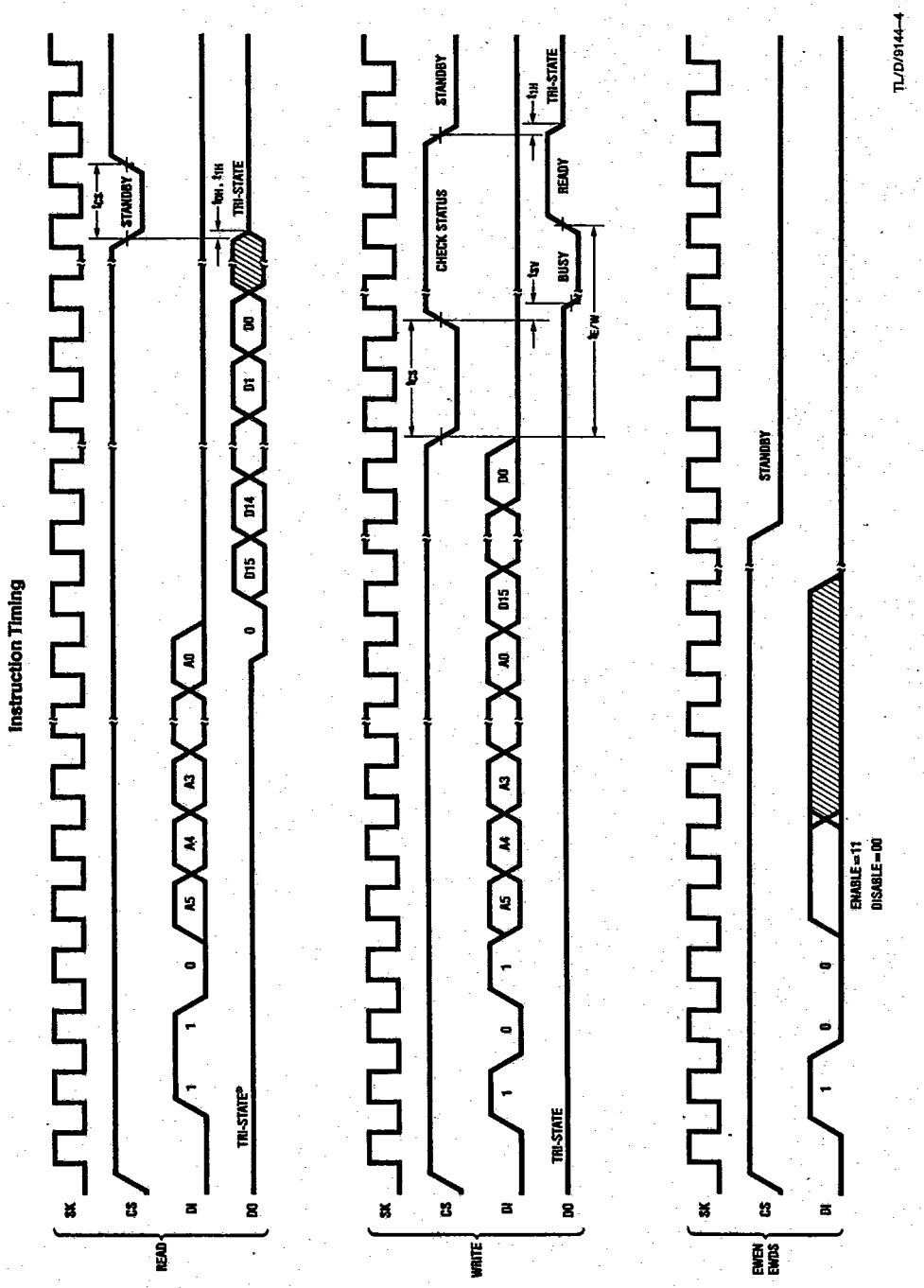

Timing Diagrams (Continued)

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